IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yoram Cedar et al.		
Assignee:	SanDisk Corporation		
Title:	Multiple Removable Non-Volatile Memory Cards Serially Communicating With a Host		
Patent No.:	6,820,148 B1	Issue Date:	November 16, 2004
Application No.:	09/641,023	Filing Date:	August 17, 2000
Examiner:	Auve, Glenn Allen	Group Art Unit:	2111
Docket No.:	SNDK.158US0	Conf. No.:	4831

Certificate of Mailing Under 37 CFR 1.8

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Mary E. Buggie

Signature

Attn: Certificate of Correction Branch Of The Patent Issue Division
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION

Sir:

Please enter the enclosed Certificate of Correction (PTO Form 1050) in the above patent.

The errors sought to be corrected were made by

☒ the Patent and Trademark Office. Thus, no fee is required for the Certificate of Correction pursuant to 37 CFR §1.322.

Please correct the following errors made by the USPTO:

Page 2, Section (56) "Other Publications", please delete the following two references:

SD Group, "SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0", dated Mar. 22, 2000, 5 pages, Items 3, 4 and 6 redacted.

SD Group, "Supplementary Notes for: SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0, Mar. 2000" dated Jan. 2000, 117 pages, Sections 4.3.5, 4.3.6, 4.3.7, 6.5 and 7 redacted.

In support of this Request, attached are copies of the Response to Office Action, Information Disclosure Statement, PTO Form 1449 and return receipt postcard, which were filed with the USPTO on March 4, 2004.

On page 4 of the Response, Applicants stated that an Information Disclosure Statement was being filed, in part, to correct the form PTO-1449 filed with the last responsive Amendment on October 9, 2003 (copy enclosed), as two SD memory card specification documents were incorrectly cited (incorrect citations are those listed above). Replacement of those citations with the corrected citations was respectfully requested. Further, on page 1 of the Information Disclosure Statement filed March 4, 2004, Applicants stated that references, numbered 5 and 6, were not being enclosed, as noted in the Response being filed with the Information Disclosure Statement. The correct citations appear on the patent. However, the above incorrect citations were also printed on the patent. Correction of this error is respectfully requested.

Column 12, line 36, claim 2:

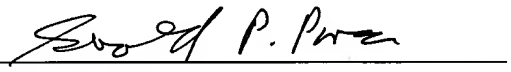
After "plurality of", delete "sockets" and insert --sockets,--.

In support of this Request, a copy of the Amendment filed May 18, 2004, showing the amendments to claim 2, is enclosed.

Because this was not an error on the part of the Applicants, Applicants believe that no fee is required. However, the Commissioner is hereby authorized to charge any fee that may be required for this correction to Deposit Account No. 502664. This form is submitted in duplicate.

Please direct all inquiries concerning this request to the undersigned attorney at (415) 318-1163.

Respectfully submitted,



April 15, 2005

Gerald P. Parsons
Reg. No. 24,486

Date

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
(415) 318-1160 (main)
(415) 318-1163 (direct)
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,820,148 B1
ISSUE DATE : November 16, 2004
INVENTOR(S) : Cedar et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 2, Section (56) "Other Publications", please delete the following references:

SD Group, "SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0", dated Mar. 22, 2000, 5 pages, Items 3, 4 and 6 redacted.

SD Group, "Supplementary Notes for: SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0, Mar. 2000" dated Jan. 2000, 117 pages, Sections 4.3.5, 4.3.6, 4.3.7, 6.5 and 7 redacted.

Column 12, line 36, claim 2:
After "plurality of", delete "sockets" and insert --sockets,--.

MAILING ADDRESS OF SENDER:

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, California 94111

PATENT NO. 6,820,148 B1
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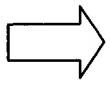

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yoram Cedar, Micky Holtzman and Yosi Pinto		
Title:	Multiple Removable Non-Volatile Memory Cards Serially Communicating With a Host		
Application No.:	09/641,023	Filing Date:	August 17, 2000
Examiner:	Auve, Glenn Allen	Group Art Unit:	2181
Docket No.:	SNDK.158Us0	Conf. No.:	4831

Certificate of Mailing Under 37 CFR 1.8

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Mary E. Buggie

Signature

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This is in response to the non-final Office Action mailed December 4, 2003, in the above-identified application. No amendments are being made.

Reconsideration of the rejection of claims 1 – 20 and 24 – 32, all the claims in the present application, is respectfully requested on the basis of the further evidence being filed herewith and the following remarks. The additional evidence is a "Supplemental Declaration of Applicants Under 37 C.F.R. § 1.132." Two identical copies of the Supplemental Declaration are being filed, one signed by one of the applicants and the other signed by the other two applicants. This Supplemental Declaration, with paragraphs 7 – 10, should be considered along with the original "Declaration of Applicants Under 37 C.F.R. § 132," filed October 9, 2003, having paragraphs 1 – 6.

In response to the rejection of all claims under 35 U.S.C. 102(a) as anticipated by the SD Specification 1.0 submitted under the provisions of MPEP §724, applicants unequivocally state in paragraph 9 of the Supplemental Declaration that the portions of the SD Specification 1.0

upon which the rejection is based as describing the claimed invention describe "subject matter conceived solely by us." This clearly satisfies the requirement of MPEP § 716.10, which states:

> "An uncontradicted 'unequivocal statement' from the applicant regarding the subject matter disclosed in an article, patent, or published application will be accepted as establishing inventorship."

In addition, the rejection under 35 U.S.C. 102(a) is believed to be improper since there has been no showing that the SD Specification 1.0 upon which the rejection is based was *publicly* known before applicants' invention. The terms "known or used" of the prior art definition of 35 U.S.C. 102(a) have been interpreted by the courts to mean "publicly" known or used. (See MPEP § 2132.) It has already been said that the SD Specification 1.0 was made available under confidence to companies joining the SDA (Original Declaration, ¶3). Indeed, a redacted version of this Specification was submitted to the USPTO in confidence under the provisions of MPEP § 724. Portions of the SD Specification 1.0 were made available to the public without restriction by a separate document (Original Declaration, ¶ 4) also submitted to the USPTO but the rejection is not based on that document. In any event, the applicants herein have been shown to be the originators of cited portions of the SD Specification 1.0.

The unequivocal statement regarding inventorship in paragraph 9 of the Supplemental Declaration is also believed to overcome the rejection under 35 U.S.C. § 102(f). Applicants have unequivocally stated that the portions of the SD Specification 1.0 relied upon in the Office Action as describing the claimed subject matter are descriptions of their invention.

The Interview Summary of examiner Glenn Auve that was mailed January 14, 2004, accurately summarizes telephone conversations had with the undersigned about this application on January 9, 12 and 13, except some additional explanation is need for the last point made in that summary. The suggestion that all portions of the SD Specification 1.0 describing the claimed subject matter or other original work of the applicants be described is believed burdensome and an unnecessary task. The techniques being claimed are not neatly described by themselves in separate sections of the document, contrary to what may be more common in other cases. Rather, they and their interaction with other portions of the memory system are described or referenced in many sections of the document. It is believed sufficient that the applicants have responded in their Supplemental Declaration concerning the sections of the SD Specification upon which the claims have been rejected in the Office Action.

To the extent that an identification of all portions of the document that describe original work of any of the applicants, even if not claimed, is being requested, this request is respectfully submitted to be totally irrelevant to any legitimate issue or factual question in this case. It is believed the added evidence being made of record by the Supplemental Declaration will satisfy the need perceived by the examiners' for additional information about the circumstances of the cited SD Specification 1.0.

The undersigned also spoke by telephone with special projects examiner Pinchus Laufer on January 14, 2004. The main topic of the telephone conversations with examiners Auve and Laufer was the adequacy of the original applicant Declaration, particularly its paragraph 6, to establish that the portions of the SD Specification 1.0 used to reject the claims are a description of applicants' invention. Paragraph 9 of the Supplemental Declaration being filed herewith supplements paragraph 6 in this regard, and directly references the rejection. In addition, as requested by the examiners, the Supplemental Declaration provides further explanations of how the subject matter described in the document was developed and the document written. In paragraph 10, Yosi Pinto declares that he was the principal writer of the SD Specification 1.0. It is believed that the concern of the examiners for a further explanation of how applicants' invention came to be described in the SD Specification 1.0 has been satisfied by the Supplemental Declaration being filed herewith.

Although this further declaration is being filed, it must be repeated that it is believed that the rejection of the claims for the lack of further information was in error. It is true that the declaration in the case of *In re DeBaun*, 687 F.2d 459, 214 USPQ 933 (CCPA 1982) included other information in addition to the unequivocal statement of inventorship but it is that statement that the court held to overcome the rejection, not the additional information included. As a result, this CCPA decision is cited by MPEP § 716.10 as authority for the USPTO policy of accepting such an unequivocal statement of inventorship to overcome such a rejection, also without mention of a need for any such additional information.

The only exception given in MPEP § 716.10 to the acceptance of an unequivocal statement of inventorship to overcome a reference describing the inventors' work is where there is some evidence that contradicts such a statement. No such contradictory evidence appears to have been asserted in either the Office Action or during the telephonic examiner interviews. The further evidence provided by the Supplemental Declaration answers the questions raised by the

examiners on account of the cited SD Specification 1.0 including contributions from other individuals at SanDisk, Toshiba and MEI. Although many individual contributions were made in the joint effort to develop specifications for the new Secure Digital (SD) memory card, those claimed in the present application are those of its applicants alone. Nothing in the present record contradicts the unequivocal statement of applicants that descriptions of the claimed subject matter in the cited SD Specification 1.0 are descriptions of inventions made solely by them.

Supplemental Information Disclosure Statement

A Supplemental Information Disclosure Statement is being filed herewith to make a few additional references of record, and to correct the form PTO-1449 filed with the last responsive Amendment on October 9, 2003. That PTO-1449 incorrectly cited the two SD memory card specification documents that have now been reviewed by the Examiner. Replacement of those citations with the corrected citations on the form PTO-1449 being filed herewith is respectfully requested. Copies of these two references are not being resubmitted.

Conclusion

For the reasons stated above, it is believed that the present application is in condition for allowance and an early indication of its allowance is solicited. However, if there are any further matters that need attention or if any questions remain, the examiner is requested to telephone the undersigned attorney at 415-318-1163.

Respectfully submitted,

Gerald P. Parsons
Reg. No. 24,486

March 4, 2004
Date

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
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(415) 693-0194 (fax)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY

Applicants:	Yoram Cedar, Micky Holtzman and Yosi Pinto		
Title:	Multiple Removable Non-Volatile Memory Cards Serially Communicating With a Host		
Application No.:	09/641,023	Filing Date:	August 17, 2000
Examiner:	Auve, Glenn Allen	Group Art Unit:	2181
Docket No.:	SNDK.158US0	Conf. No.:	4831

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Mary S. Bruggi

Signature

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

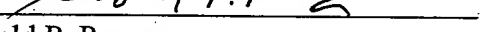
Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed, except for reference numbers 5 and 6, as noted in the Response being filed herewith.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(c). A check including $180.00 for the information disclosure statement fee under 37 C.F.R. § 1.17(p), is enclosed. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664.

Respectfully submitted,



March 4, 2004
Date

Gerald P. Parsons
Reg. No. 24,486

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San Francisco, CA 94111
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.158US0	09/641,023
	Applicants	**Conf. No.**
(Use several sheets if necessary)	Yoram Cedar et al.	4831
	Filing Date	**Art Group**
	August 17, 2000	2181

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	5,303,201	Apr. 12, 1994	Sakamoto			
	2	5,696,928	Dec. 9, 1997	Grewe et al.			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	3	JP8006892	01/12/1996	Japan			Abstract	X

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	4	CompactFlash Association, "CF+ and Compact Flash Specification, Revision 1.4", July, 1999, pp. 1-105.
Corrected Citation	5	SD Group, "SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0", dated March 22, 2000, 117 pages, Sections 4.3.5, 4.3.6, 4.3.7, 6.5 and 7 redacted.
Corrected Citation	6	SD Group, "Supplementary Notes for: SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0, March 2000" dated June 2000, 5 pages, Items 3, 4 and 6 redacted.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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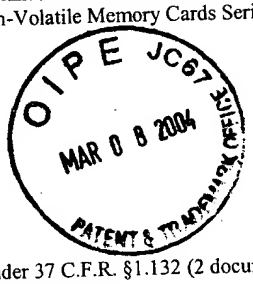
Applicants:	Yoram Cedar, Micky Holtzman and Yosi Pinto
Title:	Multiple Removable Non-Volatile Memory Cards Serially Communicating with a Host
Application No.:	09/641,023
Filing Date:	August 17, 2000
Conf. No.:	4831
Atty Docket No.:	SNDK.158US0



ENCLOSED:

1. This Return Receipt Postcard
2. Transmittal Letter (1 page - in duplicate)
3. Response to Office Action (~~4~~ 9 pages)
4. Supplemental Declaration of Applicants Under 37 C.F.R. §1.132 (2 documents - 4 pages total)
5. Supplemental Information Disclosure Statement (2 pages)
6. PTO Form 1449 (1 page)
7. Copies of 4 cited references
8. Check for $180.00

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U.S. Department of Commerce, Patent and Trademark	**Atty. Docket No.**	**Application No.**
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.158US0	09/641,023
	Applicants	**Conf. No.**
(Use several sheets if necessary)	Yoram Cedar et al.	4831
	Filing Date	**Art Group**
	August 17, 2000	2181

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Incorrect Citation	1	SD Group, "SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0", dated March 22, 2000, 5 pages, Items 3, 4 and 6 redacted.
Incorrect Citation	2	SD Group, "Supplementary Notes for: SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 1.0, March 2000" dated June 2000, 117 pages, Sections 4.3.5, 4.3.6, 4.3.7, 6.5 and 7 redacted.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yoram Cedar et al.		
Title:	Multiple Removable Non-Volatile Memory Cards Serially Communicating With a Host		
Application No.:	09/641,023	Filing Date:	August 17, 2000
Examiner:	Auve, Glenn Allen	Group Art Unit:	2111
Docket No.:	SNDK.158US0	Conf. No.:	4831

Mail Stop Amendment
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Alexandria, VA 22313-1450

AMENDMENT

Sir:

This is in response to the non-final Office Action dated May 5, 2004.

Claim Amendments are reflected in the listing of claims, which begins on page 2 of this paper.

There are no amendments to the specification or drawings.

Remarks begin on page 11 of this paper.

CLAIM AMENDMENTS

Please amend claims 1, 2, 16 and 20, as indicated on the following listing of all the claims in the present application after this Amendment:

1. (currently amended) In a system including a host and a plurality of sockets in which electronic circuit cards are mechanically inserted and electrically connected, a method of operating the system, comprising:

transferring data between the host and a card addressed over a command circuit connected between the host and the plurality of sockets, said data being transferred through a data circuit also connected between the host and the plurality of sockets, and

normally transferring commands that control operation of the electronic circuit cards from the host to an individual card over the command circuit connected between the host and the plurality of sockets except when unique addresses of the individual cards are being defined by communication between the host and the cards one at a time over the command circuit that is ~~alternatively~~ alternately connected to one of the plurality of sockets at a time.

2. (currently amended) ~~The method of claim 1, further~~ In a system including a host and a plurality of sockets in which electronic circuit cards are mechanically inserted and electrically connected, a method of operating the system, comprising:

transferring data between the host and a card addressed over a command circuit connected between the host and the plurality of sockets, said data being transferred through a data circuit also connected between the host and the plurality of sockets,

normally transferring commands that control operation of the electronic circuit cards from the host to an individual card over the command circuit connected between the host and the plurality of sockets except when unique addresses of the individual cards are being defined by communication between the host and the cards one at a time over the command circuit that is alternately connected to one of the plurality of sockets at a time,

storing within at least some of the electronic circuit cards a characteristic of a number of data contacts thereof through which data are ~~transferrable~~ transferable in parallel,

causing the host to read the stored characteristic from the cards inserted into the plurality of sockets, and

wherein transferring data between the host and an addressed card includes transferring data over one or more of a plurality of data lines connecting the host with the plurality of sockets according to the characteristic stored in the addressed card.

3. (previously presented) The method of claim 2, wherein the host provides a clock signal to the plurality of sockets to operate electronic circuit cards inserted therein with a common clock frequency regardless of the number of lines over which data are simultaneously transferred with the individual cards that are inserted into the sockets.

4. (original) The method of any one of claims 1-3, wherein the electronic circuit cards include re-writeable non-volatile memory in which the transferred data are stored.

5. (previously presented) In a system including a host and at least one socket in which at least one of a plurality of electronic circuit cards is removably insertable at one time to form an electrical connection with contacts of the card, a method of operating the system, comprising:

storing within the individual electronic circuit cards a characteristic of a number of data contacts thereof through which data are transferable in parallel,

causing the host to read the stored characteristic from said at least one card inserted into said at least one socket, and

transferring data between the host and said at least one inserted card over one or more of a plurality of lines connecting the host with said at least one socket according to the characteristic stored in said at least one inserted card.

6. (previously presented) The method of claim 5, wherein the host provides a clock signal to said at least one socket to operate said at least one inserted card with a common clock frequency regardless of the number of lines over which data are simultaneously transferred therewith.

7. (original) The method of either one of claims 5 or 6, wherein the electronic circuit cards include re-writeable non-volatile memory in which the transferred data are stored.

8. (original) The method of claim 7, wherein the host determines whether said one inserted card is a MMC type, and, if so, transfers data over only one of the plurality of data lines to said at least one socket.

9. (original) The method of claim 7, wherein transferring data between the host and said at least one inserted card includes directing individual bits of a serial data stream in sequence through a number of said data lines corresponding to the characteristic stored in said one inserted card.

10. (previously presented) A memory system, comprising:

(A) a plurality of encapsulated memory cards that individually include:

a programmable non-volatile memory and a controller of the memory,

a plurality of electrical contacts on an outer surface of the card, at least one of the contacts carrying data to and from the memory, only one of the contacts receiving commands to control operation of the controller and memory and sending a response, and a contact to receive a clock signal that operates the controller and memory, and

a plurality of registers that are programmable by command signals received through the command/response contact and readable by response signals sent through the command/response contact, including a programmable address register,

(B) a plurality of sockets which individually receive one of the plurality of cards, said sockets individually including:

at least a first pin positioned to connect with said at least one data contact of a card inserted therein, the first pins of the individual plurality of sockets being connected together into a common at least one data line,

a second pin positioned to connect with said only one command/response contact of a card inserted therein, the second pins of the individual sockets being connected into individual command/response lines,

a third pin positioned to connect with said clock signal contact of a card inserted therein, the third pins of the plurality of sockets being connected together into a common clock signal line, and

(C) a host device connected to send and receive data on said at least one common data line, to send a clock signal on the common clock signal line, and to normally simultaneously send operating commands to and receive response signals from an individual one of the cards over all of the individual command/response lines simultaneously by including an address of said individual card, except when distinct addresses in the address registers of the plurality of cards are being confirmed through one of the individual command/response lines at a time.

11. (original) The memory system of claim 10, wherein said at least one common data line includes two or more data lines, the memory cards individually provide a response of the number of contacts that carry data to and from the card memory, this response of cards inserted into the plurality of sockets being readable by the host over the command/response lines, said host being connected to transfer data with the individual memory cards inserted in each of the plurality of sockets over one or more of the two or more data lines determined by the response numbers read by the host from the respective cards.

12. (original) The memory system of claim 11, the clock signal on the common clock signal line has a frequency that remains the same without regard for the number of the two or more data lines over which data are transferred with the individual memory cards.

13. (original) A memory system, comprising:

a plurality of cards individually having a plurality of external contacts including at least one contact through which data are transferred into and out of a re-writeable non-volatile memory within the card, only one contact through which commands are received to operate the

memory and response signals sent from the memory, and a contact to receive a clock signal to operate the memory,

a plurality of sockets into which said cards are individually insertable with their contacts electrically contacting a plurality of corresponding pins including at least one data pin, only one pin for command and response signals and a clock signal pin,

a host system having a single line carrying command and response signals that is selectively connectable by the host to the command and response signal pin of any one or all of the individual card sockets, said host system additionally having at least one line that is connected with said at least one data pin of each of the plurality of sockets to carry data to and from cards inserted therein, said host system also including a clock signal line connected with said clock signal pin of each of the plurality of sockets,

said plurality of cards individually including an address register into which an address of the card is confirmed to be unique by the host through the command and response line connected to a single card at a time through the command and response pin of the card socket in which the single card is inserted, and

said host sending additional commands to and receiving additional response signals from an individual one of the cards through said command and response line when connected to the command and response pins of all of the plurality of sockets by sending on the command and response line the address stored in the address register of said individual one of the cards.

14. (original) A memory system, comprising:

a plurality of cards individually having a plurality of external contacts including one or more contacts through which data are transferred into and out of a re-writeable non-volatile memory within the card, a contact through which commands are received to operate the memory and response signals sent from the memory, and a contact to receive a clock signal to operate the memory,

a plurality of sockets into which said cards are individually insertable with their contacts electrically contacting a plurality of corresponding pins including two or more data pins, a pin for command and response signals and a pin for the clock signal,

a host system having a line carrying card command and response signals between it and the command and response pin of the plurality of sockets, a line carrying a clock signal of constant frequency over a line connected with said clock signal pin of each of the plurality of sockets, and two or more data carrying lines being connected with the two or more data pins of each of the plurality of sockets,

said plurality of cards individually having stored an indication of the number of contacts through which data are simultaneously transferrable, said stored indication being readable by the host over the command and response line, and

said host transferring data with the individual cards inserted into the plurality of sockets according to the indication stored in the individual cards.

15. (original) The memory system of claim 14, wherein the host system includes a single line carrying command and response signals that is selectively connectable by the host to the command and response signal pin of any one or all of the individual card sockets, said plurality of cards individually including an address register into which an address of the card is confirmed to be unique by the host through the command and response line to a single card at a time when connected to the command and response pin of the card socket in which the single card is inserted, and said host sending additional commands to and receiving additional response signals from an individual one of the cards through said command and response line when connected to the command and response pins of all of the plurality of sockets by sending on the command and response line the address stored in the address register of said individual one of the cards.

16. (currently amended) An enclosed card including re-writeable non-volatile memory that has a plurality of contacts including a first group of one or more contacts through which data are simultaneously ~~transferrable~~ transferable between the memory and an external host, a second group of one or more contacts receiving commands from an external host to operate the memory and ~~sending~~ send signals to an external host of the status of the operation of the memory, a third group of one or more contacts receiving a clock signal from which the memory operates, a register field that permanently stores an indication of the number of contacts

within the first group, and an interface circuit connected to read data from and write data to the memory though the number of contacts of the first group according to the stored indication.

17. (previously presented) The card of claim 16, wherein the card is 32 millimeters long, 24 millimeters wide and either 1.4 or 2.1 millimeters thick.

18. (original) A plurality of cards, each according to claim 16, wherein the number of contacts in the first group and the corresponding stored indication include at least two different numbers.

19. (original) The plurality of cards of claim 18, where in said at least two different numbers include one and four.

20. (currently amended) An enclosed card including re-writeable non-volatile memory that has a plurality of contacts including a first group of one or more contacts through which data are simultaneously ~~transferrable~~ transferable between the memory and an external host, a second group of one or more contacts receiving commands from an external host to operate the memory and ~~sending~~ send signals to an external host of the status of the operation of the memory, a third group of one or more contacts receiving a clock signal from which the memory operates, a register field that stores an address of the card that is readable by the host through the first group of contacts, and a random number generator that writes the card address into said register field.

21.-23. (canceled)

24. (previously presented) A memory card, comprising:

an enclosure,

a re-writeable non-volatile memory within the enclosure,

a plurality of electrical contacts on an outside of the enclosure that are electrically connected with said memory therein, including a group of one or more contacts through which

data are simultaneously transferable to and from said memory, at least one contact through which commands are transferable to said memory, and at least another contact through which a clock signal is received from which said memory operates, and

means including electronic circuitry within the enclosure for providing an indication through at least one of the group of data contacts of the number of data contacts within said group through which data are simultaneously transferable to and from said memory.

25. (previously presented) The memory card of claim 24, additionally comprising:

means including an interface circuit within the enclosure that is responsive to the indication means electronic circuitry for reading data from and writing data to said memory though the indicated number of contacts of said group through which data are simultaneously transferable to and from said memory.

26. (previously presented) The memory card of claim 24, wherein the indication means electronic circuitry includes a register field storing the indication of the number of data contacts within said group through which data are simultaneously transferable to and from said memory.

27. (previously presented) In a system including a host and at least one socket for removably receiving an electronic circuit card to form an electrical connection between the host and external contacts of the circuit card, a method of operating the system, comprising:

inserting a circuit card containing rewritable non-volatile memory into said at least one socket,

thereafter initializing communication between the host and the inserted circuit card including interrogation of the card by the host to determine a number of one or more of the contacts of the circuit card through which data are transferable, and

thereafter transferring data between the host and the rewritable non-volatile memory within the circuit card in parallel through the determined number of one or more circuit card contacts through which data are transferable.

28. (previously presented) The method of claim 27, wherein interrogation of the card by the host includes the host reading a register within the card to determine the number of one or more circuit card contacts through which data are transferable.

29. (previously presented) The method of claim 28, wherein the host reads the card register through one of the card contacts through which data are transferable.

30. (previously presented) The method of claim 29, wherein the number of card contacts through which data are transferable is either only said one of the card contacts or a number of two or more of the card contacts including said one of the card contacts.

31. (previously presented) The method of claim 27, wherein the host determines that data are transferable with the circuit card through only one of the circuit card contacts.

32. (previously presented) The method of claim 27, wherein the host determines that data are transferable with the circuit card through two or more of the circuit card contacts.

REMARKS

In response to dependent claims 2 and 3 being indicated as allowable, claim 2 has been rewritten in independent form. Claim 3 remains dependent upon claim 2. Formal corrective amendments have also been made to a few words of claims 1, 16 and 20.

Reconsideration of the rejection of claims 1 and 4 as anticipated under 35 U.S.C. § 102(b) by U.S. patent no. 5,491,804 ("Heath") is respectfully requested. The claim limitation that the command circuit is "connected to one of the plurality of sockets at a time" (claim 1, last line) when unique addresses are being set in the individual cards appears to have been overlooked in the Office Action. An illustration of this is shown in Figure 4 of the present application.

The function of the "address factor" AD stored in the register 21 of each card in Heath is not completely understood but appears to identify the portion of the overall system address space allocated to the individual card. In any event, the contents of register 21 of a particular card are loaded by the host over the bus 17, which is connected with all the card sockets 2-0 through 2-7 at all times. See Heath, Figure 1. An individual card is selected to receive data for its register 21 from the bus 17 by selecting one of the card enable lines EC0 – EC7 connected to that card. See Heath, col. 3, lns. 42-48. This use of the card enable lines EC0 – EC7 to enable communication of one of the cards 5-0 through 5-7 at a time with the common bus 17 is quite different from the claimed technique of connecting a command circuit to one card socket at a time.

The distinction between these different approaches has already been described in the present application. See application "Summary of the Invention," specifically p. 5, lns. 15 – 18. The selective connection of the command circuit to the individual card sockets, as claimed, allows the resulting card to be backward compatible with the MMC card. This would not be the case if the card enable signals of the Heath reference were added to the single command circuit of the prior art system shown in the present application Figure 3.

The cited Heath reference also describes permanent I/O card identification numbers (IDs) that are hard-wired during manufacture. See Heath, col. 1, ln. 27, and col. 3, ln. 9. These are not relevant to the present claims since they are not at all definable.

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters

that need to be resolved, a telephone call to the undersigned attorney at 415-318-1163 would be appreciated.

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Respectfully submitted,

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